CLAIMS:

1. An electronic circuit comprising:

first and second pipeline stages; and

a latch positioned between the pipeline stages;

wherein the electronic circuit is adapted to operate in a normal mode in which the latch is opened and closed in response to an enable signal, and a reduced mode in which the latch is held open to reduce a current peak associated with the opening and closing of the latch.

2. An electronic circuit as claimed in claim 1, further comprising a latch control circuit connected to the latch, the latch control circuit being adapted to control the latch with the enable signal when the electronic circuit is in the normal mode, and to hold the latch open when the electronic circuit is in the reduced mode.

3. An electronic circuit as claimed in claim 1, the electronic circuit further comprising a third pipeline stage and a second latch, the second latch positioned between the second and third pipeline stages.

4. An electronic circuit as claimed in claim 3, wherein, when the electronic circuit is operating in the reduced mode, both of the first and second latches are held open to reduce the current peaks associated with the opening and closing of the latches.

5. An electronic circuit as claimed in claim 3, wherein, when the electronic circuit is operating in the reduced mode, one of the first and second latches is held open to reduce the current peak associated with the opening and closing of that latch.

6. An electronic circuit as claimed in claim 5, wherein the latch held open changes over time.

7. An electronic circuit as claimed in claim 6, wherein the first and second latches are held open for different lengths of time.

8. An electronic circuit as claimed in any preceding claim, wherein the length of time that the electronic circuit operates in the reduced mode varies.

9. An electronic circuit as claimed in claim 3, further comprising a second latch control circuit connected to the second latch.

10. An electronic circuit as claimed in claim 9, wherein the latch control circuits receive a signal indicating the mode of operation of the electronic circuit.

11. An electronic circuit as claimed in claim 10, wherein the signal indicates whether the first latch, second latch or both latches are to be held open when the electronic circuit is operating in the reduced mode.

12. An electronic circuit as claimed in claim 9, wherein each latch control circuit receives a respective control signal, indicating whether its respective latch is to be held open when the electronic circuit is operating in the reduced mode.

13. A method of operating an electronic circuit, the electronic circuit comprising first and second pipeline stages and a latch positioned between the stages, the method comprising:

operating the electronic circuit in a normal mode in which the latch is opened and closed in response to an enable signal, and a reduced mode in which the latch is held open to reduce a current peak associated with the opening and closing of the latch.

14. A method as claimed in claim 13, the electronic circuit further comprising a third pipeline stage and a second latch, the second latch positioned between the second and third pipeline stages; the method further comprising:

holding the second latch open when the electronic circuit is operating in the reduced mode to reduce a current peak associated with the opening and closing of the second latch.

15. A method as claimed in claim 14, wherein the first latch and second latch are held open at different times when the electronic circuit is operating in the reduced mode.

16. A method as claimed in claim 15 wherein the first latch and second latch are held open for different lengths of time.

17. A method as claimed in claim 14, wherein, when the electronic circuit is operating in the reduced mode, both the first latch and second latch are held open.

18. A method as claimed in claim 13 wherein the length of time that the electronic circuit operates in the reduced mode varies.